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APPLICATION NO.	FILING	DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,474	01/10/2002		Leonid Baraz	42390.P8254	6444
8791	7590	06/16/2005		EXAM	INER
	SOKOLOFF	CHOW, CHIH CHING			
SEVENTH I		VARD	ART UNIT	PAPER NUMBER	
LOS ANGE	LES, CA 900	25-1030		2192	
				DATE MAIL ED. 04/14/200	· •

Please find below and/or attached an Office communication concerning this application or proceeding.

<u> </u>							
	Application No.	Applicant(s)					
	10/043,474	BARAZ ET AL.					
Office Action Summary	Examiner	Art Unit					
	Chih-Ching Chow	2192					
The MAILING DATE of this communication Period for Reply	appears on the cover sheet v	vith the correspondence address					
A SHORTENED STATUTORY PERIOD FOR RE THE MAILING DATE OF THIS COMMUNICATIO - Extensions of time may be available under the provisions of 37 CFF after SIX (6) MONTHS from the mailing date of this communication - If the period for reply specified above, the maximum state - If NO period for reply is specified above, the maximum state - Failure to reply within the set or extended period for reply will, by st - Any reply received by the Office later than three months after the mearned patent term adjustment. See 37 CFR 1.704(b).	NN. R 1.136(a). In no event, however, may a reply within the statutory minimum of th riod will apply and will expire SIX (6) MC atule, cause the application to become b	a reply be timely filed airty (30) days will be considered timely. DNTHS from the mailing date of this communication. ABANDONED (35 U.S.C. § 133).					
Status		•					
1) Responsive to communication(s) filed on 1	4 March 2005.						
	This action is non-final.						
3) Since this application is in condition for allowance except for formal matters, prosecution as to the ments is							
closed in accordance with the practice und	closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims							
4) ⊠ Claim(s) 1-27 is/are pending in the applicat 4a) Of the above claim(s) is/are withe 5) ☐ Claim(s) is/are allowed. 6) ⊠ Claim(s) 1-27 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction an	drawn from consideration.						
Application Papers							
9) The specification is objected to by the Exam	niner.						
10)⊠ The drawing(s) filed on <u>08 April 2002</u> is/are: a)⊠ accepted or b)□ objected to by the Examiner.							
Applicant may not request that any objection to	the drawing(s) be held in abeya	ance. See 37 CFR 1.85(a).					
Replacement drawing sheet(s) including the cor		·					
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for fore a) All b) Some * c) None of: 1. Certified copies of the priority docum 2. Certified copies of the priority docum 3. Copies of the certified copies of the papplication from the International Bur * See the attached detailed Office action for a	ents have been received. ents have been received in priority documents have been reau (PCT Rule 17.2(a)).	Application No n received in this National Stage					
Attachment(s)	•						
1) ☑ Notice of References Cited (PTO-892) 2) ☑ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) ☑ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/Paper No(s)/Mail Date 05/09/02.	Paper No	Summary (PTO-413) (s)/Mail Date Informal Patent Application (PTO-152) 					

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DETAILED ACTION

1. This action is responsive to amendment dated March 14, 2005.

2. Per Applicants' request, Claims 1, 10, and 19 have been amended. Claims 1-27 remain pending.

Response to Amendment

Rejection Under 35 USC § 103 4.

Applicants' amendment dated 03/14/2005, responding to the 11/09/2004 Office action provided in the 35 USC § 103 rejection for Claims 1-27. The Examiner has reviewed the amended Claims respectively. The Examiner is maintaining the 35 USC 103 rejections with additional art, i.e., "Shebanow" applied herein.

5. The Examiner is maintaining the 35 USC 103 Rejections. For the Applicants' convenience the rejections along with the amended claims are listed below.

Claim Rejections - 35 USC § 103

- The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all 6. obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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7. Claims 1, 2, 4-6, 9-11, 13-15, 18-20, 22-24 are rejected under 35
U.S.C. 103(a) as being unpatentable over US2003/0079210, by Peter Markstein et al. (hereinafter "Markstein"), in view of 'An Experimental Study of Several

Cooperative Register Allocation and Instruction Scheduling Strategies',

International Symposium on Microarchitecture, Proceedings of the 28th annual international symposium on Microarchitecture, pages 169-179, 1995; by Cindy

Norris and Lori L. Pollock. (hereinafter "Pollock"), and further in view of U.S.

Patent No. 5,355, 457 by Shebanow et al. (art made of record, hereinafter "Shebanow").

CLAIM

1. A machine-implemented method comprising:

analyzing one or more instructions of a program; and

modifying the program to use an expanded register set for a routine in the program transparently to execution of the routine.

Markstein / Pollock / Shebanow Markstein teaches the feature of analyzing a program, in Markstein, paragraph 48, "the entire source code is analyzed to generate a control flow graph" (analyzing instructions of a program); Markstein also teaches 'expand a register set', in paragraph 6, last two sentences, "A prologue and epilog typically includes code executed before and after a subroutine or program. For example, when a prologue is executed stack space may be allocated for saving necessary context, such as saving callee-saved registers. When an epilog is executed, the compiler may restore any necessary registers."; in paragraph 51, "Additional register allocation may be needed if a single intermediate level instruction expands into more than one target level instruction". Markstein teaches all aspects of claim 1, but he does not

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mention 'modifying program' and 'transparently to execution of the routine' specifically, however, Pollock teaches it in an analogous prior art. In Pollock's page 169, under '1. Introduction', second sentence, "A scheduler that rearranges code within a basic block (a routine in the program) in isolation of the rest of the program is called a local scheduler; a scheduler that moves instructions across basic blocks by considering the effects of code movement on a global level is called a global scheduler" (modifying the program). Shebanow teaches 'transaparently to execution of the routine', see Shebanow's column 7, lines 12-17, "During this allocation process, any physical registers previously assigned to these destination logical registers are unmapped, and the unmapped physical registers become 'allocated invisible' registers. Upon instruction completion ('retirement') the allocated invisible registers are returned to the free pool, and the process continues." - the invisible registers mean they are allocated transparent to the execution of the instructions.

It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Markstein's disclosure of the analyzing program and expanding registers by modifying program taught by Pollock, for

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the purpose of optimizing compilers for supporting instruction level parallelism (Pollock page 169, under 'Introduction', first sentence). Also it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Markstein's disclosure of the analyzing program and expanding registers by using invisible registers taught by Shebanow, for the purpose of using a register inventory system to monitor the allocation state changes of each of the physical registers in a register file. (Sebanow's Abstract).

2. The method of claim 1, comprising: identifying one or more register moves for the expanded register set; and modifying the program to perform the identified one or more register moves.

For the feature of claim 1 see claim 1 rejection. In Markstein paragraph 9, "identifying an operand from the intermediate code to store in a real register; and selecting an appropriate class of real registers to store the operand." See claim rejection 1 has for 'modifying program' feature.

4. The method of claim 1, wherein the modifying the program comprises modifying the program to expand a register set for a callee routine of the program.

For the feature of claim 1 see claim 1 rejection. Again, in Markstein paragraph 51, "Additional register allocation may be needed if a single intermediate level instruction expands into more than one target level instruction", the additional register (expand register set) can be for a callee routine or a caller routine. See Markstein, paragraph 27, "Different classes of real registers may include caller-saved registers. Callee-saved

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registers are preferably used to store local variables and stack items", also in the same paragraph, "A program may be compiled such that a library routine may store a temporary computation in a caller-saved register. Local variables and stack items, which are generally needed for a longer period of time, are stored in callee-saved registers (for a callee routine of the program)".

- 5. The method of claim 4, comprising: modifying the program to expand a register set for a caller routine that is to call the callee routine.
- For the feature of claim 4 see claim 4 rejection. In Markstein's disclosure cited in claim 4 rejection, it covers both callee routine and caller routine, and the caller routine can call the callee routine.
- 6. The method of claim 5, wherein the modifying the program to expand a register set for the callee routine comprises modifying the program to expand a register set that includes one or more registers of the register set for the caller routine.
- For the feature of claim 5 see claim 5 rejection. For the rest of the claim 6 feature see claim 4 rejection.

9. The method of claim 1, comprising: modifying the program to store and/or use data in one or more registers added to the register set to help analyze execution of the program.

See claim 1 rejection.

10. A machine-readable medium having instructions that, if executed by a machine, cause the machine to perform a method comprising:

Markstein's FIG. 4 shows a 'machine-readable' medium as cited in claim 10. For the rest of the features see claim 1 rejection.

analyzing one or more instructions of a

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of the routine.

program; and
modifying the program to use an
expanded register set for a routine in
the program transparently to execution

11. The machine-readable medium of claim 10, wherein the method comprises: identifying one or more register moves for the expanded register set; and modifying the program to perform the identified one or more register moves.

For the feature of claim 10 see claim 10 rejection. For the rest of the features see claim 2 rejection.

13. The machine-readable medium of claim 10, wherein the modifying the program comprises modifying the program to expand a register set for a callee routine of the program.

For the feature of claim 10 see claim 10 rejection. For the rest of the features see claim 4 rejection.

14. The machine-readable medium of claim 13, wherein the method comprises: modifying the program to expand a register set for a caller routine that is to call the callee routine.

For the feature of claim 13 see claim 13 rejection. For the rest of the features see claim 5 rejection.

15. The machine-readable medium of claim 14, wherein the modifying the program to expand a register set for the callee routine comprises modifying the program to expand a register set that includes one or more registers of the register set for the caller routine.

For the feature of claim 14 see claim 14 rejection. For the rest of the features see claim 6 rejection.

18. The machine-readable medium of claim 10, wherein the method comprises: modifying the program to store and/or

For the feature of claim 10 see claim 10 rejection. For the rest of the features see claim 9 rejection.

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use data in one or more registers added to the register set to help analyze execution of the program.

19. A system comprising:

a processor to execute instructions; and

a medium having instructions to analyze one or more instructions of a program and to modify the program to use an expanded register set for a routine in the program transparently to execution of the routine.

20. The system of claim 19, the medium having instructions to identify one or more register moves for the expanded register set and to modify the program to perform the identified one or more register moves.

22. The system of claim 19, the medium having instructions to modify the program to expand a register set for a callee routine of the program.

23. The system of claim 22, the medium having instructions to modify the program to expand a register set for a caller routine that is to call the callee routine.

24. The system of claim 23, the medium having instructions to modify the program to expand a register set that includes one or more registers of the register set for the caller routine.

Same as claim 10 rejection.

For the feature of claim 19 see claim 19 rejection. For the rest of the features see claim 2 rejection.

For the feature of claim 19 see claim 19 rejection. For the rest of the features see claim 4 rejection.

For the feature of claim 22 see claim 22 rejection. For the rest of the features see claim 5 rejection.

For the feature of claim 23 see claim 23 rejection. For the rest of the features see claim 6 rejection.

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8. Claims 3, 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US2003/0079210, by Peter Markstein et al. (hereinafter "Markstein"), in view of 'An Experimental Study of Several Cooperative Register Allocation and Instruction Scheduling Strategies', International Symposium on Microarchitecture, Proceedings of the 28th annual international symposium on Microarchitecture, pages 169-179, 1995; by Cindy Norris and Lori L. Pollock. (hereinafter "Pollock"), further in view of U.S. Patent No. 5,355, 457 by Michael Shebanow et al. (hereinafter "Shebanow"), and further in view of U.S. Patent No. 5,644,709 by Todd Michael Austin (hereinafter "Austin").

CLAIM

- 3. The method of claim 2, wherein the identifying comprises:
- (a) defining one or more move chains for the expanded register set, and
- (b) identifying a sequence of one or more register moves based on the defined one or more move chains.

Markstein / Pollock/ Shebanow /Austin

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For the feature of claim 2 see claim 2 rejection. In Pollock page 169, under 'Introduction', "Register allocation techniques are either local, global, or interprocedural depending on whether the allocator attempts an assignment of registers to values within basic blocks (chain) in isolation of other basic blocks, across basic blocks of a procedure, or across procedure boundaries, respectively." The 'identifying register' feature is the 'register allocation' recited in Pollock's prior art, see claim rejection 1. Pollock teaches register allocation of claim 3, but he does not mention 'move chain' specifically, however, Austin teaches it in an analogous prior art. In Austin column 7, lines 19-26, "A call-chain is the state of the stack at some point in a program's execution; it is composed of a sequence

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of function names; functions higher in the call-chain call (possibly indirectly) the functions lower in the call chain; neighbors in the call-chain share a direct caller-callee relationship. A partial call-chain is a subset of the current complete call-chain, usually taken from the bottom of the complete call chain; partial call-chains are usually employed to reduce storage requirements."

It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to supplement Markstein's and Pollock's disclosures of the analyzing program and expanding registers by call chain taught by Austin, for the purpose of adjusting the appropriate counts at calls (Austin column 7, lines 34-35) thus no callee routine would be left out during a program rearrangement.

- 12. The machine-readable medium of claim 11, wherein the identifying comprises:
- (a) defining one or more move chains for the expanded register set, and
- (b) identifying a sequence of one or more register moves based on the defined one or more move chains.
- 21. The system of claim 20, the medium having instructions to define one or more move chains for the expanded register set and to identify a sequence

For the feature of claim 11 see claim 11 rejection. For the rest of the features see claim 3 rejection.

For the feature of claim 20 see claim 20 rejection. For the rest of the features see claim 3 rejection.

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of one or more register moves based on the defined one or more move chains.

Conclusion

- 9. The following summarizes the status of the claims: 35 USC § 103 rejection: Claims 1-27
- 10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chih-Ching Chow whose telephone number is 571-272-3693. The examiner can normally be reached on 7:30am - 4:00pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Any inquiry of a general nature of relating to the status of this application should be directed to the **TC2100 Group receptionist**: **571-272-2100**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chih-Ching Chow

Examiner

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June 9, 2005

CC

TUAN DAM SUPERVISORY PATENT EXAMINER